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AC LINE FREQUENCY DIVIDERS

January 2003

RED SERIES

RED 5/6 Divide by 5 or 6 RED 50/60 Divide by 50 or 60 RED 100/120 Divide by 100 or 120 RED 300/360 Divide by 300 or 360 Divide by 500 or 600 RED 500/600 RED 3000/3600 Divide by 3000 or 3600

FEATURES:

- Clock input pulse shaper accepts 50Hz/60Hz sine wave directly
- · Fully static counter operation
- +4.5V to +15V operation (VDD VSS)
- Low power dissipation
- · High noise immunity
- Reset
- Input Enable
- 50Hz/60Hz division select input
- Output low power TTL compatible at +4.5V operation
- Square Wave Output (except for ÷ 5)
- RED x/y (DIP); RED x/y-S (SOIC) See Figure 1

APPLICATION:

Time base generator from either 50 Hz or 60 Hz line frequency to produce:

10 pulses per second	(RED 5/6)
1 pulse per second	(RED 50/60)
1 pulse per 2 seconds	(RED 100/120)
1 pulse per .1 minute	(RED 300/360)
1 pulse per 10 seconds	(RED 500/600)
1 pulse per minute	(RED 3000/3600)

DESCRIPTION OF OPERATION:

The counter advances by one on each negative transition of the input clock pulse as long as the Enable signal is High and the Reset signal is Low. When the Enable signal is Low the input clock pulses will be inhibited and the counter will be held at the state it was in prior to bringing the Enable Low. A High Reset signal clears the counter to zero count.

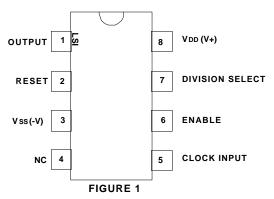
Depending on the device used, a Low on the Division Select input will cause a Divide by 6, 60, 120, 360, 600 or 3600. A High on the Division Select will cause a Divide by 5, 50, 100, 300, 500 or 3000.

All outputs are 50% duty cycle except RED 5, where output is low for two clocks and high for three clocks.

CLOCK INPUT

If input signals are less than the Vss or greater than VDD, a series input resistor should be used to limit the maximum input current to 2 mA.

PIN ASSIGNMENT - TOP VIEW



MARKING AS FOLLOWS: **MARKING** PART

RED 5/6	RED 6
RED 50/60	RED 60
RED 100/120	RED 120
RED 300/360	RED 360
RED 500/600	RED 600

MAXIMUM RATINGS:

RED 3000/3600

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperatur	re Ta	-40 to +85	°C
DC Supply Voltage	(VDD - Vss)	+18	V
Voltage at any input	Vin	Vss - 0.3 to VDD + 0.3	V

RED 3600

ENABLE SIGNAL TIMING

If the Enable signal switches Low during a positive clock phase and then switches High during a negative clock phase, a false count will be registered. To prevent this from happening, the Enable signal should not switch Low during a positive clock phase unless the switch to High also occurs during a positive clock phase. The Enable signal should normally be switched during a negative clock phase.

> The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

`	TA = 25° u	ınless c	therwise s	pecified)	Clock Rise and Fall Time:	V DD 5V		MAX mum Limit	UNITS
EST CONDITIONS: Vss = OV Output Cap	oacitance	Load	= 15 pF		Clock Frequency	10V 5V	DC	mum Limit 600	- KHz
Input Rise a except cloc	and Fall t	times :	= 20 ns,			10V	DC	1200	KHz
nput Capacitance = 5pF max (ar	ny input) VDD	Min	Max	Units	Input Clock Pulse Width	5V 10V	800 400	-	ns ns
Quiescent Device Current	5V 10V	-	10 20	uA uA	Output Rise and Fall Time	5V	_	225	ns
Output Voltage, Low Level	5V 10V	-	0.0 0.0	V V	Output Nise and Fair Fillio	10V	-	150	ns
High Level	5V	4.99	-	V	Propagation Delay to Output	5V	-	1500	ns
lock Input Voltage, Low Level	10V 5V	9.99	1	V		10V	-	750	ns
High Level	10V 5V	4	2	V V	Enable Set-up Time	5V 10V	-	300 150	ns ns
nput Noise Immunity (except clock)	10V 5V	8 1.5	-	V V	Reset Pulse Width	5V	800	_	ns
(Low and High) Output Drive Current	10V	3.0	-	V	Nosci also widai	10V	400	-	ns
N Channel Sink Current (Vout = Vss +0.4V)	4.5V 10V	0.18 0.45	-	mA mA	Reset Removal Time	5V	-	1200	ns
ange P Channel Sink Current	4.5V	0.3	_	mA		10V	-	600	ns
(Vout = VDD -1)	10V	0.3	-	mA	Reset Propagation Delay to Output	5V 10V	-	1400 700	ns ns
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	.							1	
PULSE SHAPER	INPU	UT CLO	OCK GENE	RATOR	ENABLE 6	\sim	~		
N 5	<u> </u>	_		►CL	RESET 2	\rightarrow	<u> </u>	— ▶ R	
	<u> </u> -		- >>	►CL	DIVISION SELECT 7	\rightarrow		→ DS	
Ē	¦ R			1 1 1	+4.5V to +15V — 8	- VDD			
	! ! !				GND — 3	– vss			
					N/C — 4				
								7	
RED 5/6,50/60. 300/360,3000/3600							1	D5/6	
							1	J	
300/360,3000/3600	CL1			012				J	
300/360,3000/3600 DS CL 3 BIT	CL1	3 BIT	SON		BIT CL3 5 BIT OHNSON CL3 JOHNSON			J	
300/360,3000/3600 DS	CL1_CL1	3 BIT JOHNS ÷10		→ 3	BIT CL3 5 BIT JOHNSON +6 +10			D50/60	00
300/360,3000/3600 DS 3 BIT JOHNSON	<u> </u>	JOHNS		3	OHNSON CL3 JOHNSON			D50/60	oo
300/360,3000/3600 DS 3 BIT JOHNSON	<u> </u>	JOHNS		3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600 DS 3 BIT JOHNSON	<u> </u>	JOHNS		3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS	CL1	JOHNS		CL2 3	OHNSON CL3 JOHNSON			D50/60	00
300/360,3000/3600 CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON DS	CL1	JOHNS ÷10	т	CL2 CL2	DHNSON +6 CL3 JOHNSON +10			D3000/360	00
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT	CL1	JOHNS ÷10	T NSON	CL2	OHNSON CL3 JOHNSON +10			D50/60	00
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON	CL1	JOHNS +10	T NSON	CL2 CL2	DHNSON +6 CL3 JOHNSON +10			D3000/360	00
300/360,3000/3600 DS 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON +5/6 R	CL1	JOHNS +10	T NSON	CL2 CL2	DHNSON +6 CL3 JOHNSON +10			D3000/360	00
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON +5/6	CL1	JOHNS +10	T NSON	CL2 CL2	DHNSON +6 CL3 JOHNSON +10			D3000/360	00
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON +5/6	CL1	5 BI JOHN ÷1	T NSON O	CL2 1 CL2	DHNSON +6 CL3 JOHNSON +10			D3000/360	00
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON +5/6 R RED 500/600 DS CL 3 BIT JOHNSON +5/6	CL1	5 Bi Johns 5 Bi John John John John John John John John	T NSON O	CL2 1 CL2 5 5 JC	DHNSON +6 BIT +2			D50/60 D3000/360 D300/360 D100/120	
300/360,3000/3600 DS CL 3 BIT JOHNSON +5/6 R RED 100/120 DS CL 3 BIT JOHNSON +5/6 R RED 500/600 DS	CL1 CL1 CL1	5 Bi Johns +11	T NSON O	CL2 1 CL2 5 5 JC	BIT +2 BIT HHNSON			D50/60 D3000/360 D300/360 D100/120	