LS8397

STEPPER MOTOR CONTROLLER

FEATURES:
- Controls Bipolar and Unipolar Motors
- L297 operation with added functions:
  - Selectable torque ripple compensated phase drive
  - Selectable automated switching between stepping and holding torques
- Supply current < 400uA
- Half and full step modes
- Normal/wave drive
- Direction control
- Reset input
- Step control input
- Enable input
- PWM chopper circuit for current control
- Two over current sensor comparators with external references input
- All inputs and outputs TTL/CMOS compatible (TTL for 5V operation)
- 4.75V to 7V Operation (Vdd – Vss).
- LS8397 (DIP), LS8397-S (SOIC), LS8397-TS (TSSOP)
  – See Figure 1 –

DESCRIPTION:

The LS8397 Stepper Motor Controller generates four phase drive signal outputs for controlling two phase Bipolar and four phase Unipolar motors. The outputs are used to drive two H-bridges for the two motor windings in the Bipolar motor or the four driver transistors for the two center-tapped windings in the Unipolar motor. The motor can be driven in full step mode either in normal drive (two-phase-on) or wave drive (one-phase-on) and half step mode. The LS8397 provides two inhibit outputs which are used to control the driver stages of each of the motor phases. The circuit uses STEP, FRD/REV and HALF/FULL inputs in a translator to generate controls for the output stages.

A dual PWM chopper circuit using an on-chip oscillator, latches and voltage comparators are used to regulate the current in the motor windings. For each pair of phase driver outputs (PHA, PHB, and PHC, PHD) each pulse of the common internal oscillator sets the latch and enables the output. If the current in the motor winding causes the voltage across a sense resistor to exceed the reference voltage, VREFs, at the comparator inputs, the latch is reset disabling the output until the next oscillator pulse.

Input for a separate reference voltage VREFh is also provided for reducing holding torque when the motor is not turning. When holding torque mode is enabled with a resistor-capacitor pair connected to the RC Pin, the sense comparator input reference switches between VREFs and VREFh depending on whether the motor is turning or not. The separate sense reference voltages allow for conserving power when the motor is not turning. Holding torque mode can be disabled by connecting the RC Pin to Vss.

In the half-step stepping sequence, the phase drives alternate between one-phase-on and two-phase-on in successive steps at full power thus generating substantial ripple on the output torque. An input, CT_EN is provided for selecting an operational mode in which the torque ripple is corrected. In this mode the sense input reference voltage is switched to 100% and 70.7% of the applied voltages at the VREFs and VREFh inputs in successive one-phase-on and two-phase-on conditions, respectively. The CONTROL input determines whether the chopper acts on the phase driver outputs or the inhibit outputs. When the phase lines are chopped, the non-active phase line of each pair (PHA, PHB or PHC, PHD) is activated rather than deactivating the active line to reduce dissipation in the load sensing resistor Rs. Refer to Figure 5B for Bipolar motors. If PHA is high and PHB is low, current flows through Q1, motor winding, Q4 and sense resistor Rs. When chopping occurs, PHB is brought high and circulating current flows through Q1 and D3 and not through Rs resulting in less power dissipation in Rs. Current decay is slow using this method. When the Control input is brought low, chopping occurs by bringing INH1 low. In this case circulating current flows through D2, motor winding and D3 and through the power supply to ground causing the current to decay rapidly. For Unipolar motors, only inhibit chopping is used. Refer to Figure 6. When INH1 is brought low the current flowing in either half of the center tapped motor winding recirculates through the diode across it.

INPUT/OUTPUT DESCRIPTION:

OSC Input
An RC input with the resistor connected to VDD and the capacitor connected to ground determines the oscillator chopper rate. When connected as an oscillator, the oscillator output appears as a negative-going pulse at the Sync pin. If the oscillating pin is tied to ground, the Sync pin becomes an input. Osc frequency, fosc = 1/0.69RC.
SYNC
As an output the sync can be used to drive sync pins of other
LS8397s. This eliminates the need for RC components for any
other LS8397 controllers used in the system. As an input the
sync can be driven by the LS8397 that has the RC oscillator
components or by any other system external clock.

PHA/PHB/PHC/PHD
Phase drive output signals for power stages. In a Bipolar motor
PHA and PHB are used for one H-bridge while PHC and PHD
are used for the other.

INH1/INH2 Outputs
These outputs are active low inhibit controls for motor drive
outputs. INH1 controls driver stage using PHA and PHB sig-
nals while INH2 control driver stage using PHC and PHD sig-
nals. When the Control input is low, these outputs are chopped
using the internal oscillator for current regulating.

CONTROL Input
When high, the phase outputs, PHA, PHB, PHC and PHD are
chopped. When low, INH1 and INH2 are chopped. Normally,
inhibit outputs are chopped. Phase chopping might be used with
a Bipolar motor that does not store much energy to pre-
vent fast current decay and a low useful torque.

ENABLE Input
When Enable input is low, INH1, INH2, PHA, PHB, PHC and
PHD are brought low.

HOME Output
An open drain output that indicates when the LS8397 is in its
initial state with PHA, PHB, PHC, PHD = logic states 0101 re-
spectively. Refer to Figure 4. In the active state the open
drain device is off.

STEP Input
An active low pulse on this input causes the motor to advance
one step. The step occurs on the rising edge of the step signal.

FRD/REV Input
A logic 1 on this input causes the motor to advance through
the stepping sequence of Fig. 4. A logic 0 on this input cause
the motor to reverse the sequence.

RESET Input
An active low on this input cause the motor to be restored to
the home position (0101).

HALF/FULL Input
When high, half-step operation is selected. When low, full-step
operation is selected. The one-phase-on full step is selected
by selecting full when the stepping sequence is at an even
state. The two-phase-on full step operation is selected when
the stepping sequence is at an odd state. Refer to Figure 4.

SENSE1/ SENSE2 Inputs
Inputs for load current sense voltages from power stages using
PHA and PHB drive signals or PHC and PHD drive signals,
respectively.

When holding-torque mode is enabled, the motor torque is
switched to stepping torque at a step command followed by
holding torque after a programmable delay. The stepping torque
is controlled by the reference voltage VREFs input and the hold-
ing torque is controlled by the voltage at the VREFh input. The
delay is controlled by a resistor-capacitor pair connected to the
RC pin.

When the holding-torque mode is disabled, the motor torque re-
mains in the stepping torque mode all the time controlled by the
VREFs voltage.

RC Input/Output
A resistor-capacitor pair connected to this pin starts a time-out
delay at every step command. At the start of the delay, the ref-
ence voltage at the VREFs pin is switched in for the SENSE
comparators to produce higher stepping torque. At the end of
the time-out, the reference voltage at the VREFh pin is switched
in for the SENSE comparators to produce the lower holding
torque, reducing power dissipation while the motor is stationary.

The delay is given by Tds = 1.4RC

If tied low, holding torque mode is disabled and stepping torque
is produced in both dynamic and static states by using the
VREFs reference voltage.

VREFs Input
Input for the SENSE comparator reference voltage for produc-
ing stepping torque.

VREFh Input
Input for the SENSE comparator reference voltage for produc-
ing holding torque.

CT_EN Input
Input for selecting/deselecting compensated torque-ripple
mode. The step sequence in the half-step mode alternates be-
 tween one-phase-on and two-phase-on states resulting in
torque ripple during the stepping sequence. In the compensat-
ed-torque mode, the ripple is eliminated by equalizing the
 torques for the alternate states. This is done by alternately
switching the SENSE reference voltages between 100% and
70.7% in alternate cycles.

The CT_EN input is relevant only in the half-step mode, since
the alternating one-step-on and two-step-on sequence does not
exist in the full-step mode.

This input has an internal pull-up.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_s)</td>
<td>Supply Voltage</td>
<td>10</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_i)</td>
<td>Input Signals</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(T_{stg}, TJ)</td>
<td>Storage and Junction Temperatures</td>
<td>-40 to +150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**ELECTRICAL CHARACTERISTICS:** (Refer to Block Diagram, Figure 2, and Timing Diagram, Figure 3)

\(T_A = +25°C\), \(V_{DD} = +5V\) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>(V_{DD})</td>
<td>4.75</td>
<td>-</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Supply Current</td>
<td>(I_{DD})</td>
<td>-</td>
<td>300</td>
<td>400</td>
<td>uA</td>
<td>Outputs floating</td>
</tr>
<tr>
<td>(Pins 13, 14, 21, 22, 23 and 24) Input Voltage Low</td>
<td>(V_{IL})</td>
<td>-</td>
<td>-</td>
<td>0.75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage High</td>
<td>(V_{IH})</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(Pins 14, 21, 22, 23, 29) Input Current</td>
<td>(I_{IH}, I_{IL})</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>nA</td>
<td>(V = V_{IL}) or (V_{IH})</td>
</tr>
<tr>
<td>Input Current (Pin 13)</td>
<td>(I_{IL})</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>nA</td>
<td>(V = 0)</td>
</tr>
<tr>
<td></td>
<td>(I_{IH})</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>nA</td>
<td>(V = V_{DD})</td>
</tr>
<tr>
<td>(Pins 4, 6, 7, 9) Phase Output Voltage Low</td>
<td>(V_{OL})</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>V</td>
<td>(I_o = -10mA)</td>
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<tr>
<td>Phase Output Voltage High</td>
<td>(V_{OH})</td>
<td>4.0</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>(I_o = 5mA)</td>
</tr>
<tr>
<td>(Pins 5, 8)</td>
<td>Inhibit Output Voltage Low</td>
<td>(V_{INL})</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>Inhibit Output Voltage High</td>
<td>(V_{INH})</td>
<td>4.0</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>(I_o = 5mA)</td>
</tr>
<tr>
<td>Leakage Current (Pin 3)</td>
<td>(I_{Leak})</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>uA</td>
<td>(V_{CE} = 7V)</td>
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<tr>
<td>Saturation Voltage (Pin 3)</td>
<td>(V_{Sat})</td>
<td>-</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
<td>(I = 5mA)</td>
</tr>
<tr>
<td>(Pins 13, 14, 15) Comparator Offset Voltage</td>
<td>(V_{O#})</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>mV</td>
<td>(V_{REF} = 1V)</td>
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<td>Comparator Bias Current</td>
<td>(I_o)</td>
<td>100</td>
<td>-</td>
<td>10</td>
<td>uA</td>
<td></td>
</tr>
<tr>
<td>(Pins 18, 19) Input Reference Voltages</td>
<td>(V_{REFs}, V_{REFh})</td>
<td>0</td>
<td>-</td>
<td>3</td>
<td>V</td>
<td>(V_{REFs}, V_{REFh} = 3V)</td>
</tr>
<tr>
<td>Input Currents</td>
<td>(I_{REFs}, I_{REFh})</td>
<td>-</td>
<td>-</td>
<td>8</td>
<td>uA</td>
<td>(V_{REFs}, V_{REFh} = 3V)</td>
</tr>
<tr>
<td>(Pin 11)</td>
<td>RC Input Low</td>
<td>(V_{RCL})</td>
<td>0</td>
<td>-</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>RC Input High</td>
<td>(V_{RCH})</td>
<td>3.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>External resistor at RC</td>
<td>(R)</td>
<td>10</td>
<td>-</td>
<td>No Limit</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Step Pulse Width</td>
<td>(t_{stp})</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>Set up time</td>
<td>(t_s)</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>Hold time</td>
<td>(t_h)</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>Reset time</td>
<td>(t_r)</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>Reset to Step delay</td>
<td>(t_{RStp})</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>(Pin 20) Oscillator:</td>
<td>Sawtooth Low</td>
<td>(V_{SOL})</td>
<td>-</td>
<td>2.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Sawtooth High</td>
<td>(V_{SOH})</td>
<td>-</td>
<td>3.65</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### LS8397 Block Diagram

**Parameter** | **Symbol** | **Minimum** | **Typical** | **Maximum** | **Unit** | **Condition**
---|---|---|---|---|---|---
Oscillator Frequency | \( f_{\text{OSC}} \) | - | 30 | - | kHz | \( R = 22k\Omega, C = 3.3nF \)
Sync Output Voltage Low | \( V_{\text{SyncL}} \) | - | - | 0.8 | V | \( I_O = -5mA \)
Sync Output Voltage High | \( V_{\text{SyncH}} \) | 3.0 | - | - | V | \( I_O = 5mA \)
Sync Input Pulse Width | \( T_{\text{SPW}} \) | - | 3.3 | - | V | \( R = 22k\Omega, C = 3.3nF \)
Sync Input Switching Point | \( T_{\text{SSP}} \) | - | 2.0 | - | us | Pin 16 \( \leq 1.0V \)
Sync Input Pulse Width | \( I_{\text{IS}} \) | - | -425 | - | uA | Pin 16 \( \leq 1.0V, V_{\text{IN}} = V_{\text{DD}} \)

**FIGURE 2. LS8397 BLOCK DIAGRAM**

**FIGURE 3. Input Timing Diagram**
FIGURE 4. MOTOR DRIVING SEQUENCES
The LS8397 generates phase sequences for half-step mode, normal drive mode and wave drive mode. Advancing occurs on the positive edge of the STEP input signal. HOME is defined as PHA, PHB, PHC, PHD being 0101, respectively. The State Diagrams showing the phase output polarities for all states are shown above for clockwise rotation. For counter clockwise rotation, the sequences are reversed. RESET restores the phases to 0101 and State 1.
FIGURE 5A. Typical Application Schematic for a Two-Phase Bipolar Motor Using a Single Motor Driver IC

Note: The SENSE resistors on L298 should be chosen so that $I_{MAX} = \frac{V_{RS}}{R_s}$, where $I_{MAX}$ is the maximum motor winding current.

FIGURE 5B. One half of L298 Drive Stage
FIGURE 6. TYPICAL APPLICATION SCHEMATIC FOR A FOUR-PHASE UNIPOLAR MOTOR USING DISCRETE MOSFET TRANSISTORS

NOTE: Q1, Q2, Q3, Q4 are MOSFET Power Transistors suitable for 5V Gate Drive
Typical P/Ns = IRLZ44N and IRF3708
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