FEATURES:

• Programmable modes are: Up/Down, Binary, BCD, 24 Hour Clock, Divide-by-N, x1 or x2 or x4 Quadrature and Single-Cycle.
• DC to 25MHz Count Frequency.
• 8-Bit I/O Bus for uP Communication and Control.
• 24-Bit comparator for pre-set count comparison.
• Readable status register.
• Input/Output TTL and CMOS compatible.
• 3V to 5.5V operation (V DD - V SS).
• LS7166 (DIP); LS7166-S (SOIC); LS7166-TS (24-Pin TSSOP) - See Figure 1 -

GENERAL DESCRIPTION:
The LS7166 is a CMOS, 24-bit counter that can be programmed to operate in several different modes. The operating mode is set up by writing control words into internal control registers (see Figure 8). There are three 6-bit and one 2-bit control registers for setting up the circuit functional characteristics. In addition to the control registers, there is a 5-bit output status register (OSR) that indicates the current counter status. The IC communicates with external circuits through an 8-bit three state I/O bus. Control and data words are written into the LS7166 through the bus. In addition to the I/O bus, there are a number of discrete inputs and outputs to facilitate instantaneous hardware based control functions and instantaneous status indication.

REGISTER DESCRIPTION:
Internal hardware registers are accessible through the I/O bus (D0 - D7) for READ or WRITE when CS = 0. The C/D input selects between the control registers (C/D = 1) and the data registers (C/D = 0) during a READ or WRITE operation. (See Table 1)
PR (Preset register). The PR is the input port for the CNTR. The CNTR is loaded with a 24 bit data via the PR. The data is first written into the PR in 3 WRITE cycle sequence of Byte 0 (PR0), Byte 1 (PR1) and Byte 2 (PR2). The address pointer for PR0/PR1/PR2 is automatically incremented with each write cycle. Accessed by: WRITE when C/D = 0, CS = 0.

<table>
<thead>
<tr>
<th>Bit #</th>
<th>7 - - - - - - - - - - 0</th>
<th>7 - - - - - - - - - - 0</th>
<th>7 - - - - - - - - - - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR2</td>
<td>(BYTE 2)</td>
<td>PR1</td>
<td>(BYTE 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PR0</td>
</tr>
</tbody>
</table>

Standard Sequence for Loading PR and Reading CNTR:
1. MCR; Reset PR address pointer
2. WRITE PR; Load Byte 0 and into PR0 increment address
3. WRITE PR; Load Byte 1 and into PR1 increment address
4. WRITE PR; Load Byte 2 and into PR3 increment address
5. MCR; Transfer PR to CNTR

MCR (Master Control Register). Performs register reset and load operations. Writing a "non-zero" word to MCR does not require a follow-up write of an “all-zero” word to terminate a designated operation. Accessed by: WRITE when C/D = 1, CS = 0.

<table>
<thead>
<tr>
<th>Bit #</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

0: Reset PR/OL address pointer
1: Transfer CNTR to OL (24 bits)
1: Reset CNTR, BWT and CYT. Set SIGN bit. (CNTR = 0, BWT = 0, CYT = 0, SIGN = 1)
1: Transfer PR to CNTR (24 bits)
1: Reset COMPT (COMPT = 0)
1: Master reset. Reset CNTR, ICR, OCR, QR, BWT, CYT, OL COMP, and PR/OL address pointer. Set PR (PR = FFFFFFF) and SIGN.

NOTE: Control functions may be combined.

ICR (Input Control Register). Initializes counter input operating modes. Accessed by: WRITE when C/D = 1, CS = 0.

<table>
<thead>
<tr>
<th>Bit #</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

0: Input A = Up count input, Input B = Down count input
1: Input A = Count input, Input B = Count direction input (overridden in quadrature mode) where B = 0 selects up count mode and B = 1 selects Down count mode.

(NOTE: During counting operation B may switch only when A = 1.)

0: NOP
1: Increment CNTR once (A/B = 1, if enabled)
0: NOP
1: Decrement CNTR once (A/B = 1, if enabled)
0: Disable inputs A/B
1: Enable inputs A/B
0: Initialize Pin 4 as CNTR Reset input (Pin 4 = RCTR)
1: Initialize Pin 4 as Enable/Disable gate for A/B inputs (Pin 4 = ABGT)
0: Initialize Pin 3 as CNTR load input (Pin 3 = LCTR)
1: Initialize Pin 3 as OL load input (Pin 3 = LLTC)
1: Select ICR
0: __

NOTE: Control functions may be combined.
TABLE 1 - Register Addressing Modes

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>C/D</th>
<th>RD</th>
<th>WR</th>
<th>CS</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Disable Chip for READ/WRITE</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write to Master Control Register (MCR)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write to input control register (ICR)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write to output/counter control register (OCCR)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write to quadrature register (QR)</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Write to preset register (PR) and increment register address counter.</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read output latch (OL) and increment register address counter</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Read output status register (OSR).</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Read output latch (OL) and increment register address counter</td>
</tr>
</tbody>
</table>

X = Don't Care

**OSR (Output Status Register).** Indicates CNTR status: Accessed by: READ when C/D = 1, CS = 0.

<table>
<thead>
<tr>
<th>Bit #</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
</tr>
</tbody>
</table>

- **BWT.** Borrow Toggle Flip-Flop. Toggles every time CNTR underflows generating a borrow.
- **CYT.** Carry Toggle Flip-Flop. Toggles every time CNTR overflows generating a carry.
- **COMPT.** Compare Toggle Flip-Flop. Toggles every time CNTR equals PR
- **SIGN.** Sign bit. Reset ( = 0) when CNTR underflows
  Set ( = 1) when CNTR overflows
- **UP/DOWN.** Count direction indicator in quadrature mode.
  Reset ( = 0) when counting down
  Set ( = 1) when counting up
  (Forced to 1 in non-quadrature mode)

**OL (Output latch).** The OL is the output port for the CNTR. The 24 bit CNTR Value at any instant can be accessed by performing a CNTR to OL transfer and then reading the OL in 3 READ cycle sequence of Byte 0 (OL0), Byte 1 (OL1) and Byte 2 (OL2). The address pointer for OL0/OL1/OL2 is automatically incremented with each READ cycle. Accessed by: READ when C/D = 0, CS = 0.

<table>
<thead>
<tr>
<th>Bit #</th>
<th>7</th>
<th>0</th>
<th>7</th>
<th>0</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OL2 (BYTE 2)</td>
<td>OL1 (BYTE 1)</td>
<td>OL0 (BYTE 0)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Standard Sequence for Loading and Reading OL:
3 → MCR; Reset OL address pointer and Transfer CNTR to OL
READ OL; Read Byte 0 and increment address
READ OL; Read Byte 1 and increment address
READ OL; Read Byte 2 and increment address
OCCR (Output Control Register)  Initializes CNTR and output operating modes.
Accessed by:  WRITE when C/D = 1, CS = 0.

Bit #  7  6  5  4  3  2  1  0

0: Binary count mode (Overridden by D3 = 1).
1: BCD count mode (Overridden by D3 = 1)

0: Normal count mode
1: Non-Recycle count mode. (CNTR enabled with a Load or Reset
   CNTR and disabled with generation of Carry or Borrow.
   In this mode no external CY or BW is generated. Instead
   CYT or BWT should be used as cycle completion indicator.)

0: Normal count mode
1: Divide by N count mode (CNTR is reloaded with PR data upon
   Carry or Borrow).

0: Binary or BCD count mode (see D0)
1: 24 Hour Clock mode with Byte 0 = Sec, Byte 1 = Min and Byte 2 = Hr.
   (Overrides BCD/Binary Modes)

0: Pin 16 = CY, Pin 17 = BW. (Active Low)
1: Pin 16 = CYT, Pin 17 = BWT

0: Pin 16 = CY, Pin 17 = BW. (Active high)
1: Pin 16 = COMP, Pin 17 = COMPT

0: Select OCCR
1: Select OCCR

QR (Quadrature Register).  Selects quadrature count mode (See Fig. 7)
Accessed by:  WRITE when C/D = 1, CS = 0.

Bit #  7  6  5  4  3  2  1  0

1 1 X X X X 1

0: Disable quadrature mode
1: Enable x1 quadrature mode

0: Enable x2 quadrature mode
1: Enable x4 quadrature mode

1: Select QR

X = Don’t Care
I/O DESCRIPTION:
(See REGISTER DESCRIPTION for I/O Programming.)

Data-Bus (D0 - D7) (Pin 8 - Pin 15). The 8-line data bus is a three-state I/O bus for interfacing with the system bus.

CS (Chip Select Input) (Pin 2). A logical "0" at this input enables the chip for Read and Write.

RD (Read Input) (Pin 19). A logical "0" at this input enables the data bus to be written into the control and data registers.

WR (Write Input) (Pin 1). A logical "0" at this input enables the data bus to be written into the control and data registers.

C/D (Control/Data Input) (Pin 18). A logical "1" at this input enables a control word to be written into one of the four control registers or the OSR to be read on the I/O bus. A logical "0" enables a data word to be written into the PR, or the OL to be read on the I/O bus.

A (Pin 6). Input A is a programmable count input capable of functioning in three different modes, such as up count input, down count input and quadrature input. In non-quadrature mode, the counter advances on the rising edge of Input A.

B (Pin 7). Input B is also a programmable count input that can be programmed to function either as down count input, or count direction control gate for input A, or quadrature input. In non-quadrature mode, and when programmed as the Down Count input, the counter advances on the rising edge of Input B. When B is programmed as the count direction control gate, B = 0 enables A as the Up Count input and B = 1 enables A as the Down Count input. When programmed as the direction input, B can switch state only when A is high.

ABGT/RCTR (Pin 4). This input can be programmed to function as either inputs A and B enable gate or as external counter reset input. A logical "0" is the active level on this input. In non-quadrature mode, if Pin 4 is programmed as A and B enable gate input, it may switch state only when A is high (if A is clock and B is direction) or when both A and B are high (if A and B are clocks). In quadrature mode, if Pin 4 is programmed as A and B enable gate, it may switch state only when either A or B switches.

LCTR/LLTC (Pin 3) This input can be programmed to function as the external load command input for either the CNTR or the OL. When programmed as counter load input, the counter is loaded with the data contained in the PR. When programmed as the OL load input, the OL is loaded with data contained in the CNTR. A logical "0" is the active level on this input.

CY (Pin 16) This output can be programmed to serve as one of the following:
A. CY. Complemented Carry out (active "0").
B. CY. True Carry out (active "1").
C. C YT. Carry Toggle flip-flop out.
D. COMPT. Comparator out (active "0").

BW (Pin 17) This output can be programmed to serve as one of the following:
A. BW. Complemented Borrow out (active "0").
B. BW. True Borrow out (active "1").
C. B WT. Borrow Toggle flip-flop out.
D. COMPT. Comparator Toggle output.

VDD (Pin 5) Supply voltage positive terminal.

VSS (Pin 20) Supply voltage negative terminal.

Absolute Maximum Ratings:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage at any input</td>
<td>VIN</td>
<td>VSS - 0.3 VDD + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>TA</td>
<td>-40 to +125</td>
<td>oC</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>TSTG</td>
<td>-65 to +150</td>
<td>oC</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>VDD - VSS</td>
<td>+7.0</td>
<td>V</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics. (All voltages referenced to Vss. TA = 0° to 85°C, VDD = 3V to 5.5V, fc = 0, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min. Value</th>
<th>Max. Value</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VDD</td>
<td>3.0</td>
<td>5.5</td>
<td>V</td>
<td>Outputs open</td>
</tr>
<tr>
<td>Supply Current</td>
<td>IDD</td>
<td>-</td>
<td>350</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>VIL</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>VIH</td>
<td>2.0</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>VOL</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
<td>4mA Sink, VDD = 5V</td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>VOH</td>
<td>2.5</td>
<td>-</td>
<td>V</td>
<td>200µA Source, VDD = 5V</td>
</tr>
<tr>
<td>Input Current</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>nA</td>
<td>Leakage Current</td>
</tr>
<tr>
<td>Output Source Current</td>
<td>ISRC</td>
<td>200</td>
<td>-</td>
<td>µA</td>
<td>VOH = 2.5V, VDD = 5V</td>
</tr>
<tr>
<td>Output Sink Current</td>
<td>ISINK</td>
<td>4</td>
<td>-</td>
<td>mA</td>
<td>VOL = 0.4V, VDD = 5V</td>
</tr>
<tr>
<td>Data Bus Off-State</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Leakage Current</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>nA</td>
<td></td>
</tr>
</tbody>
</table>
### Transient Characteristics

(See Timing Diagrams in Fig. 2 thru Fig. 7, VDD = 3V to 5.5V, TA = 0˚ to 85˚C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min. Value</th>
<th>Max. Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock A/B &quot;Low&quot; TCL</td>
<td>18</td>
<td>No Limit</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Clock A/B &quot;High&quot; TCH</td>
<td>22</td>
<td>No Limit</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Clock A/B Frequency fc</td>
<td>0</td>
<td>25</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>(See NOTE 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock UP/DN Reversal Delay TUDD</td>
<td>100</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>LCTR Positive edge to the next A/B positive</td>
<td>TLC</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>or negative edge delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock A/B to CY/BW/COMP &quot;low&quot; propagation</td>
<td>TCBL</td>
<td>-</td>
<td>65</td>
<td>ns</td>
</tr>
<tr>
<td>delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock A/B to CY/BW/COMP &quot;high&quot; propagation</td>
<td>TCBH</td>
<td>-</td>
<td>85</td>
<td>ns</td>
</tr>
<tr>
<td>delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCTR and LLTC pulse width TLCW</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Clock A/B to CYT, BWT and COMPT &quot;high&quot;</td>
<td>TTFH</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>propagation delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock A/B to CYT, BWT and COMPT &quot;low&quot;</td>
<td>TTFL</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>propagation delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WR pulse width TWR</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>RD to data out delay (CL=20pF) TR</td>
<td>-</td>
<td>110</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CS, RD Terminate to</td>
<td>TRT</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Data-Bus Tri-State</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data-Bus set-up time for WR TDS</td>
<td>30</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data-Bus hold time for WR TDH</td>
<td>30</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS set-up time for RD TSRS</td>
<td>0</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS hold time for RD TSRH</td>
<td>0</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Back to Back RD delay TRR</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>RD to WR delay -</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>C/D set-up time for RD TCRS</td>
<td>0</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>C/D hold time for RD TCRH</td>
<td>30</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>C/D set-up time for WR TCWS</td>
<td>30</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>C/D hold time for WR TCWH</td>
<td>30</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS set-up time for WR TSWS</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS hold time for WR TSWH</td>
<td>0</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Back to Back WR delay TWW</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>WR to RD delay -</td>
<td>60</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Quadrature Mode:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock A/B Validation delay TCQV</td>
<td>-</td>
<td>160</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(See NOTE 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A and B phase delay TPH</td>
<td>208</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Clock A/B frequency fc FCQ</td>
<td>-</td>
<td>1.2</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>CY, BW, COMP pulse width TCBW</td>
<td>85</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 1:** In quadrature mode A/B inputs are filtered and required to be stable for at least TCQV length to be valid.
FIGURE 2. LOAD COUNTER, UP CLOCK, DOWN CLOCK, COMPARE OUT, CARRY, BORROW

NOTE 1: The counter in this example is assumed to be operating in the binary mode.
NOTE 2: No COMP output is generated here, although PR = CNTR. COMP output is disabled with a counter load command and enabled with the rising edge of the next clock, thus eliminating invalid COMP outputs whenever the CNTR is loaded from the PR.
NOTE 3: When UP Clock is active, the DN Clock should be held “HIGH” and vice versa.

FIGURE 3. CLOCK TO CY/BW OUTPUT PROPAGATION DELAYS
FIGURE 4. READ/WRITE CYCLES

FIGURE 5. DIVIDE BY N MODE

FIGURE 6. CYCLE ONCE MODE
FIGURE 7.
QUADRATURE MODE INTERNAL CLOCKS
FIGURE 8.
LS7166 BLOCK DIAGRAM
Figure 9. 80C31/8051 to LS7166 Interface in External Address Mode

NOTE: Port_0 is open drain output. Add pull-up resistors to all Port_0 i/o lines.
FIGURE 10. 8751 INTERFACE TO LS7166 IN I/O MODE
FIGURE 11. LS7166 TO 68HC11 INTERFACE
FIGURE 12. LS7166 INTERFACE EXAMPLE

ISA BUS

D7
D6
D5
D4
D3
D2
D1
D0

AEN

A8
A7
A6
A5
A4
A3
A2
A1

A0

IOR/
IOW/

ADDRESS DECODER

D0
D1
D2
D3
D4
D5
D6
D7

LS7166

D0
D1
D2
D3
D4
D5
D6
D7

WR
RD
C/D
CS

1
19

IOW/

18

A0

2
FIGURE 13. 68000 INTERFACE TO LS7166

DATA BUS

ADDRESS

D Q
LS373
CK

A0

DECODE

D0 - D7

C/D

CS

RD

WR

R/W

LDS/UDS

68000
68008
68010

AS

DTACK

CLK

CLOCK

D S
S74

CK R Q

S D
S74

Q CK R

7166

+V

+V
C Sample Routines for Interfacing with LS7166

#include <stdio.h>
#include <stdlib.h>
#include <conio.h>

#define DATAMODE(arg) (arg + 0)
#define CTRLMODE(arg) (arg + 1)

/***********************/
/* MCR (Master Control Register) */
/***********************/
/* Select MCR */
#define MCR(arg) (arg | 0x00)
/* Master Reset */
/* Reset CNTR, ICR, OCCR, QR, BWT, CYT, OL, COMPT, and PR/OL Byte Pointer */
/* Set PR and SIGN */
#define Rst_Master 0x20
/* Reset COMPT */
#define Rst_COMPT 0x10
/* Transfer PR to CNTR (24 bits) */
#define Trf_PR_CNTR 0x08
/* Reset CNTR, BWT and CYT */
/* Set SIGN bit */
#define Rst_CNTR_BWT_CYT_Set_SIGN 0x04
/* Transfer CNTR to OL (24 bits) */
#define Trf_CNTR_OL 0x02
/* Reset PR/OL Byte Pointer */
#define Rst_BP 0x01

/***********************/
/* ICR (Input Control Register) */
/***********************/
/* Select ICR */
#define ICR(arg) (arg | 0x40)
/* Select LCTR / LLTC as Load-CNTR Input */
#define LCNTR 0x00
/* Select LCTR / LLTC as Load-OL Input */
#define LOL 0x20
/* Select ABGT / RCTR as Reset-CNTR Input */
#define RCNTR 0x00
/* Select ABGT / RCTR as Enable / Disable Gate for A / B Inputs */
#define ABGate 0x10
/* Disable A / B Inputs */
#define DisAB 0x00
/* Enable A / B Inputs */
#define EnAB 0x08
/* Decrement CNTR once for A / B = 1, if A / B inputs are enabled */
#define Decr_CNTR 0x04

/* Increment CNTR once for A / B = 1, if A / B inputs are enabled */
#define Incr_CNTR 0x02

/* Set Input A = Up Count Input, Input B = Down Count Input */
#define AUP_BDN 0x00

/* Set Input A = Count Input, Input B = Count Direction Input */
/* B = 0 selects Up Count Mode */
/* B = 1 selects Down Count Mode */
#define AIN_BDIR 0x01

/*************************************************************************/
/* OCCR (Output Control Register) */

/* Select OCCR */
#define OCCR(arg) (arg | 0x80)

/* Set CY = COMP Comparator Out (active "0") */
/* Set BW = COMPT Comparator Toggle Output */
#define COMPN_COMPT 0x30

/* Set CY = CY */
/* Set BW = BW */
#define CY_BW 0x20

/* Set CY = CY */
/* Set BW = BW */
#define CYN_BWN 0x00

/* Set Binary or BCD Count Mode */
#define Bin_BCD_Cnt 0x00

/* Set 24 Hr Clock Mode – Overrides BCD / Binary Modes */
#define Clk_24HR_Cnt 0x08

/* Set Normal Count Mode */
#define Nrml_Cnt 0x00

/* Set Divide by N Count Mode */
#define div_N_Cnt 0x04

/* Set Non Recycle Count Mode */
#define Nrcyc_Cnt 0x02

/* Set Binary Count Mode */
#define Bin_Cnt 0x00

/* Set BCD Count Mode */
#define BCD_Cnt 0x01

/*************************************************************************/
/* QR (Quadrature Register) */
/* Select QR */
#define QR(arg) (arg | 0xC0)

/* Enable x4 Quadrature Mode */
#define En_x4QM 0x03

/* Enable x2 Quadrature Mode */
#define En_x2QM 0x02

/* Enable x1 Quadrature Mode */
#define En_x1QM 0x01

/* Disable Quadrature Mode */
#define Dis_QM 0x00

/************************************************************************/
/* Initialize 7166 */

void Init_7166(int Addr)

/* Initialize 7166 as follows
Do a Master Reset
Set ICR as follows
Set Input A = Up Count
Set Input B = Down Count
Disable Inputs A/B
Enable Reset_CNTR input
Enable Load_CNTR input
Set OCCR – Normal Count Mode
Disable QM
Enable A and B Inputs */

void Init_7166(int Addr){
/* Master Reset */
outp(CTRLMODE(Addr), MCR(Rst_Master));

/* Set ICR */
outp(CTRLMODE(Addr), ICR(AUP_BDN + DisAB + RCNTR + LCNTR));

/* Set OCCR */
outp(CTRLMODE(Addr), OCCR(Nrml_Cnt));

/* Set QR */
outp(CTRLMODE(Addr), QR(Dis_QM));

/*Enable A and B inputs */
outp(CTRLMODE(Addr), ICR(EnAB));
}
/* Write data into 7166 Preset Register  
Addr has address of 7166 counter  
Data has 24 bit data to be written to PR register */

void Write_7166_PR(int Addr, unsigned long Data);

void Write_7166_PR(int Addr, unsigned long Data)
{
    outp(CTRLMODE(Addr), MCR(Rst_BP));
    outp(DATAMODE(Addr), (unsigned char)Data);
    Data >>= 8;
    outp(DATAMODE(Addr), (unsigned char)Data);
    Data >>= 8;
    outp(DATAMODE(Addr), (unsigned char)Data);
}

/* Read 7166 Output Latch  
Addr has address of 7166 counter  
Data returns 24 bit OL register value. */

unsigned long Read_7166_OL(int Addr);

unsigned long Read_7166_OL(int Addr)
{
    unsigned long Data = 0;
    outp(CTRLMODE(Addr), MCR(Rst_BP + Trf_CNTR_OL));
    Data |= (unsigned long) inp(DATAMODE(Addr));
    lrot(Data,8);
    Data |= (unsigned long) inp(DATAMODE(Addr));
    lrot(Data,8);
    Data |= (unsigned long) inp(DATAMODE(Addr));
    lrot(Data,16);
    return(Data);
}

/* Read Output Status Register  
Addr has address of 7166 counter  
returns OSR data */

unsigned long Read_7166_OSR(int Addr);

unsigned long Read_7166_OSR(int Addr)
{
    return(inp(CNTRLMODE(Addr)));
}