

QUADRATURE CLOCK CONVERTER

January 2009

FEATURES:

- x1 and x4 mode selection
- Up to 16MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +4.5V to +10V operation ($V_{DD} - V_{SS}$)
- LS7083, LS7084 (DIP);
LS7083-S, LS7084-S (SOIC) - See Figure 1

Applications:

- Interface incremental encoders to Up / Down Counters (See Figure 6A and Figure 6B)
- Interface rotary encoders to Digital Potentiometers (See Figure 7)

DESCRIPTION

The **LS7083** and **LS7084** are CMOS quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the **LS7083** or **LS7084**, are converted to strings of Up Clocks and Down Clocks (**LS7083**) or to a Clock and an Up/Down direction control (**LS7084**). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the en-

INPUT/OUTPUT DESCRIPTION:

RBIAS (Pin 1)

Input for external component connection. A resistor connected between this input and VSS adjusts the output clock pulse width (T_{OW}). For proper operation, the output clock pulse width must be less than or equal to the A, B pulse separation ($T_{OW} \leq T_{PS}$).

V_{DD} (Pin 2)

Supply Voltage positive terminal.

V_{SS} (Pin 3)

Supply Voltage negative terminal.

A (Pin 4)

Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

B (Pin 5)

Quadrature Clock Input B. This input has a filter circuit identical to input A.

x4/x1 (Pin 6)

This input selects between x1 and x4 modes of operation. A high-level selects x4 mode and a low-level selects the x1 mode. In x4 mode, an output pulse is generated for every transition at either A or B input. In x1 mode, an output pulse is generated in one combined A/B input cycle. (See Figure 2.)

PIN ASSIGNMENT - TOP VIEW

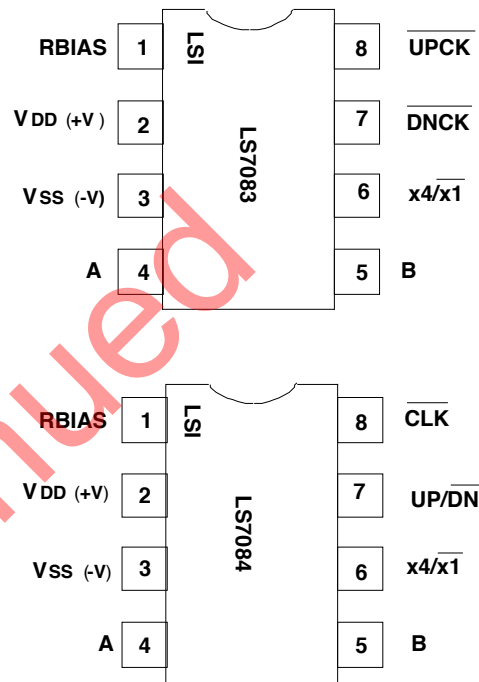


FIGURE 1

LS7083 - \overline{DNCK} (Pin 7)

In LS7083, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

LS7084 - $\overline{UP/DN}$ (Pin 7)

In LS7084, this is the count direction indication output. When A input leads the B input, the $\overline{UP/DN}$ output goes high indicating that the count direction is UP. When A input lags the B input, $\overline{UP/DN}$ output goes low, indicating that the count direction is DOWN.

LS7083 - \overline{UPCK} (Pin 8)

In LS7083, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

LS7084N - \overline{CLK} (Pin 8)

In LS7084, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the $\overline{UP/DN}$ output (Pin 7).

NOTE: For the **LS7084**, the timing of \overline{CLK} and $\overline{UP/DN}$ requires that the counter interfacing with **LS7084** counts on the rising edge of the \overline{CLK} pulses.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	V _{DD} - V _{SS}	11.0	V
Voltage at any input	V _{IN}	V _{SS} - 0.3 to V _{DD} + 0.3	V
Operating temperature	T _A	0 to +70	°C
Storage temperature	T _{STG}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:(All voltages referenced to V_{SS}, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	V _{DD}	4.5	10.0	V	-
Supply current	I _{DD}	-	6.0	μA	V _{DD} = 10V, All input frequencies = 0Hz RBIAS = 2M
x4/x1 Logic Low	V _{IL}	-	0.3V _{DD}	V	-
A, B Logic Low	V _{IL}	-	0.6	V	V _{DD} = 4.5V
		-	1.0	V	V _{DD} = 9V
		-	1.1	V	V _{DD} = 10V
x4/x1 Logic High	V _{IH}	0.7V _{DD}	-	V	-
A, B Logic High	V _{IH}	3.1	-	V	V _{DD} = 4.5V
		5.0	-	V	V _{DD} = 9V
		5.6	-	V	V _{DD} = 10V
ALL OUTPUTS:					
Sink Current	I _{OL}	1.75	-	mA	V _{DD} = 4.5V
VoL = 0.4V		5.0	-	mA	V _{DD} = 9V
		5.7	-	mA	V _{DD} = 10V
Source Current	I _{OH}	1.0	-	mA	V _{DD} = 4.5V
VoH = V _{DD} - 0.5V		2.5	-	mA	V _{DD} = 9V
		3.0	-	mA	V _{DD} = 10V

TRANSIENT CHARACTERISTICS:(T_A = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
A, B inputs: Validation Delay	T _{VD}	-	85	ns	V _{DD} = 10V
		-	100	ns	V _{DD} = 9V
		-	160	ns	V _{DD} = 4.5V
A, B inputs: Pulse Width	T _{PW}	T _{VD} + T _{OW}	Infinite	ns	-
A to B or B to A Phase Delay	T _{PS}	T _{OW}	Infinite	ns	-
A, B frequency	f _{A, B}	-	$\frac{1}{2T_{PW}}$	Hz	-
Input to Output Delay	T _{DS}	-	120	ns	V _{DD} = 10V
		-	150	ns	V _{DD} = 9V
		-	235	ns	V _{DD} = 4.5V Includes input validation delay
Output Clock Pulse Width	T _{OW}	50	-	ns	See Fig. 4 & 5

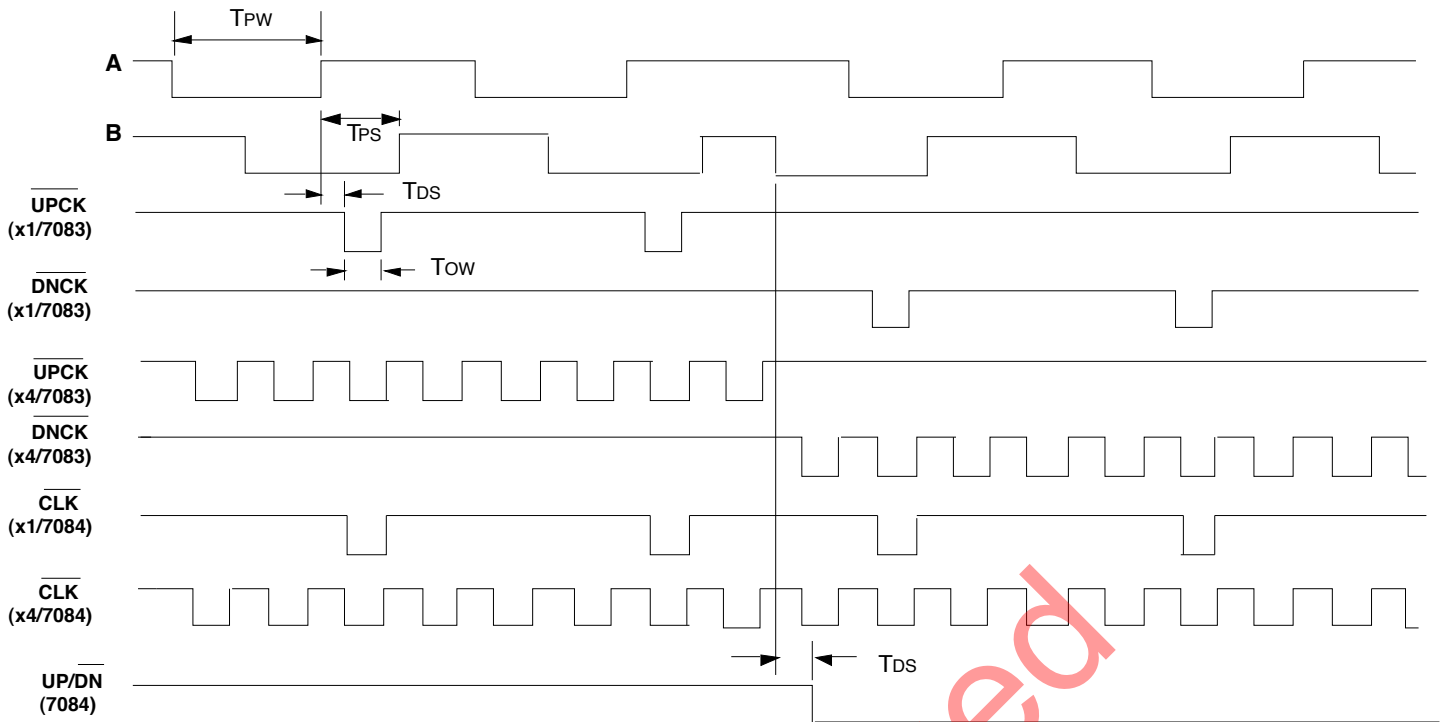


FIGURE 2. LS7083 / LS7084 INPUT / OUTPUT TIMING DIAGRAM

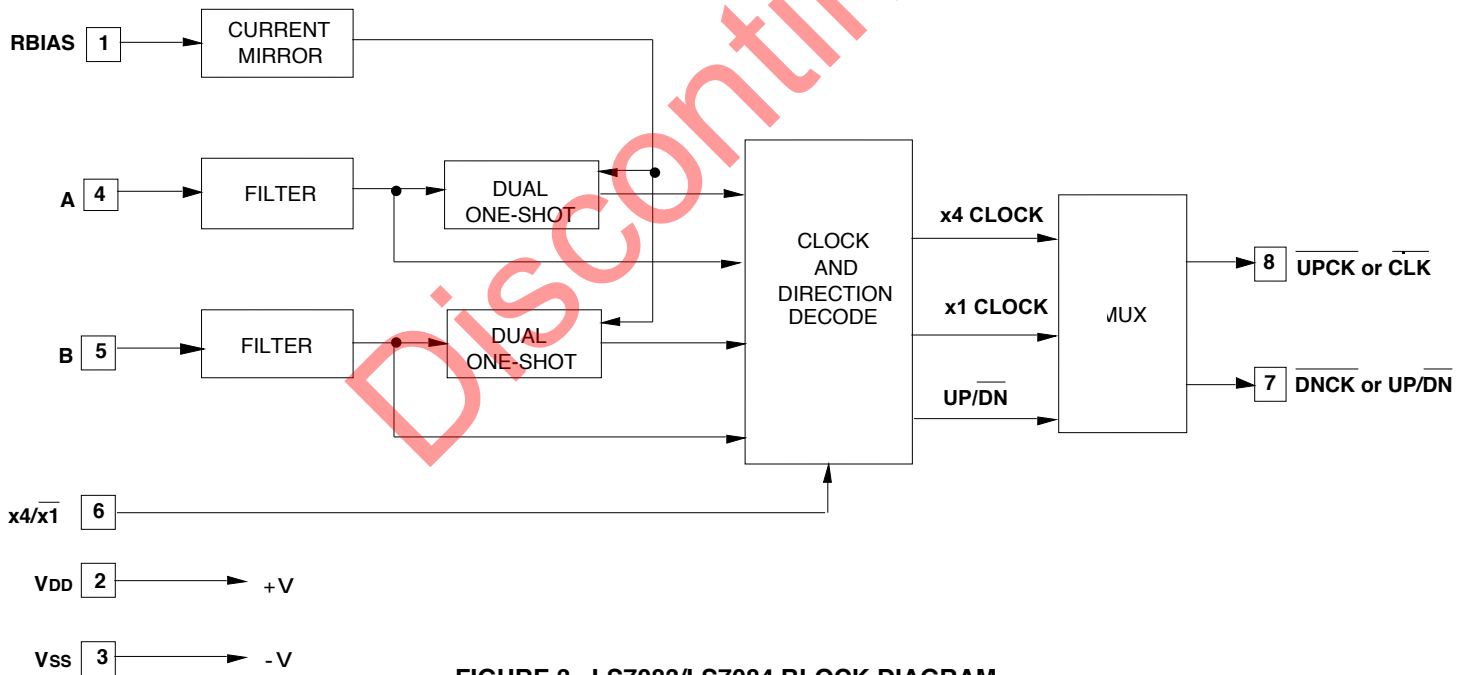


FIGURE 3. LS7083/LS7084 BLOCK DIAGRAM

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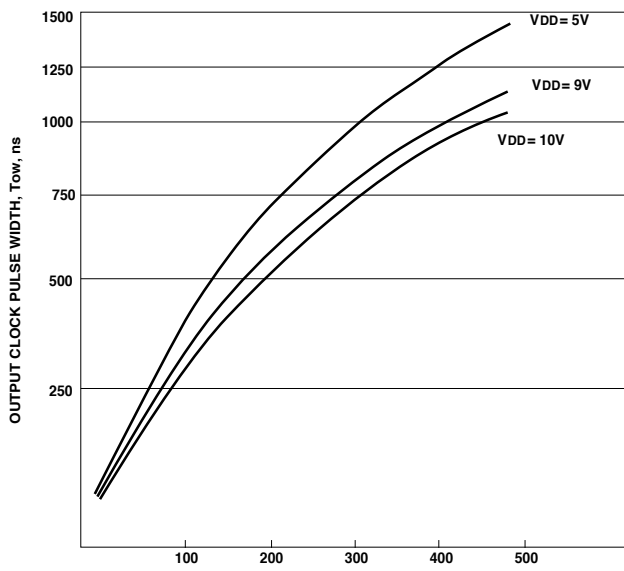


Figure 4. Tow vs RBIAS, kΩ

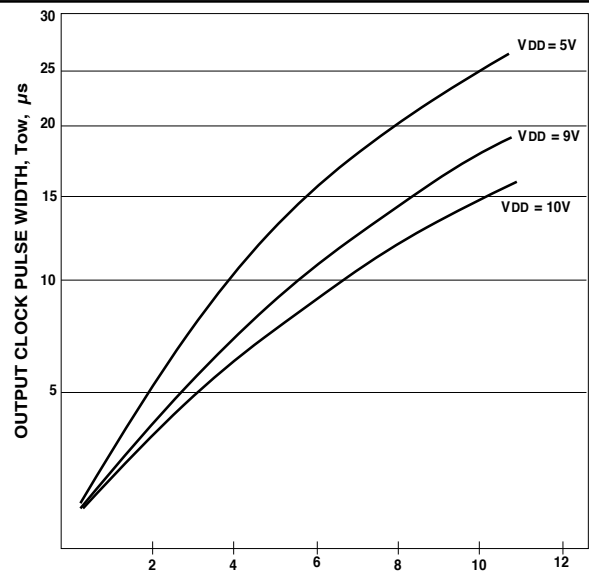


Figure 5. Tow vs RBIAS, MΩ

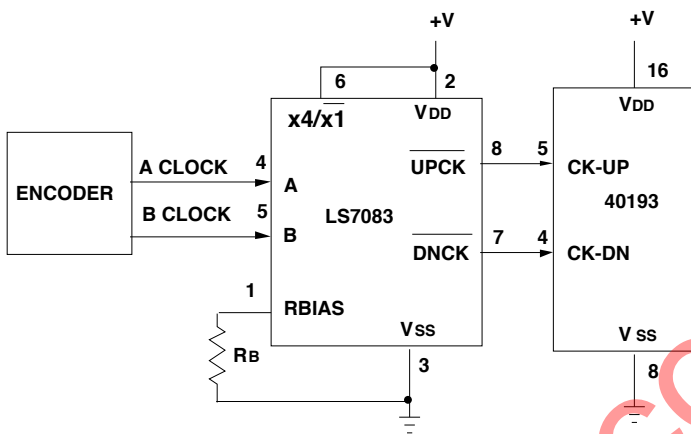


FIGURE 6A. TYPICAL APPLICATION FOR LS7083 IN x4 MODE

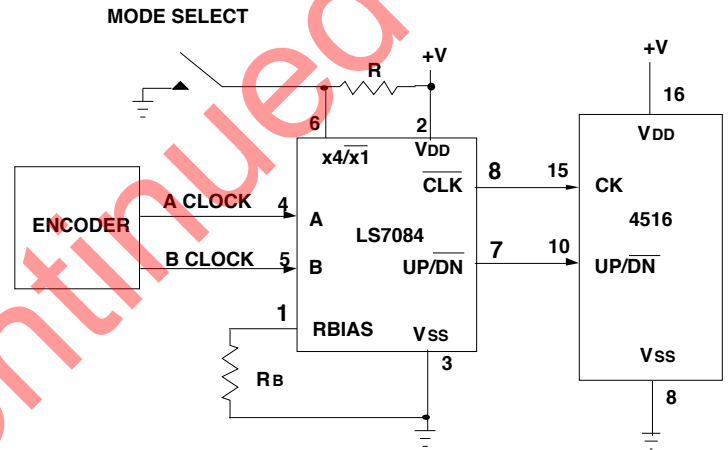
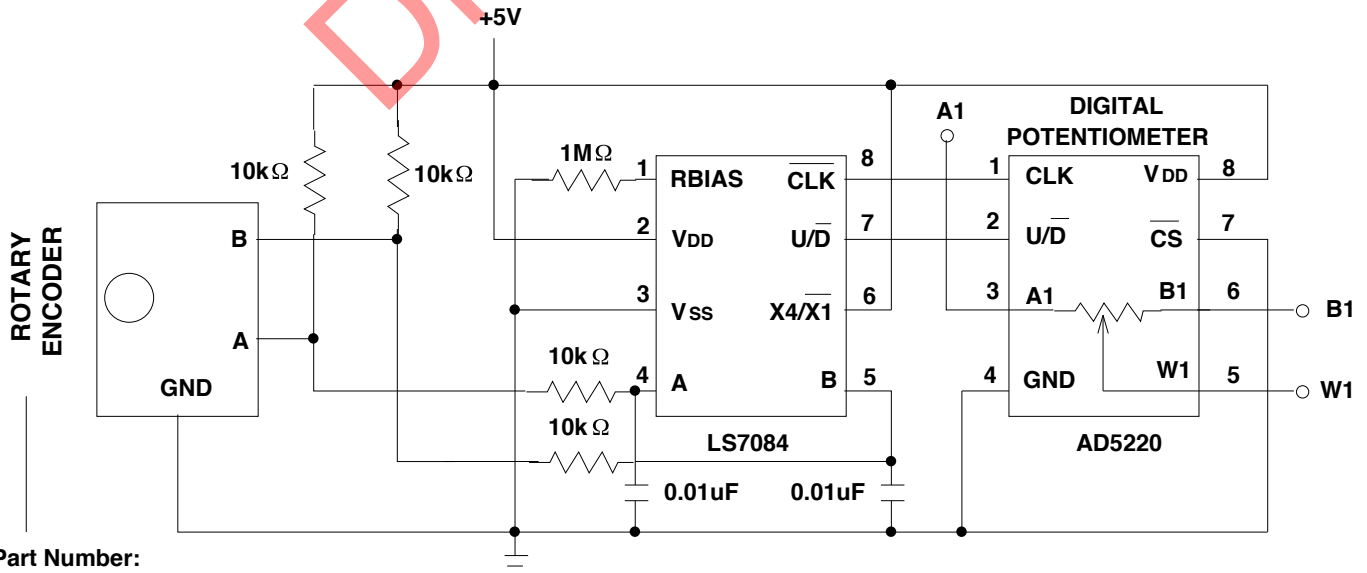


FIGURE 6B*. TYPICAL APPLICATION FOR LS7084 WITH X4/X1 MODE SELECTION

*See NOTE at bottom right of Page 1



Part Number:
RE11CT-V1Y12-EF2CS

FIGURE 7. Rotary Encoder Control of Digital Potentiometer