

QUADRATURE CLOCK CONVERTER

FEATURES:

- X1 and x4 mode selection
- Up to 16MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications
- TTL and CMOS compatible I/Os
- +3V to +12V operation ($V_{DD} - V_{SS}$)
- LS7083NS-14 (SOIC) – See Figure 1.

Applications:

- Interface incremental encoders to Up/Down Counters (See Figure 6A and 6B)

DESCRIPTION:

The LS7083NS-14 is a CMOS quadrature clock converter. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the LS7083NS-14 are converted to strings of Up Clocks and Down Clocks. These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

V_{DD} (Pin 2)

Supply voltage positive terminal.

RBIAS (Pin 3)

Input for external component connection. A resistor connected between this input and V_{SS} adjusts the output clock pulse width (T_{OW}). For proper operation, the output clock pulse width must be less than or equal to the A, B pulse separation ($T_{OW} \leq T_{PS}$).

V_{SS} (Pin 4)

Supply voltage negative terminal.

A (Pin 5)

Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

B (Pin 10)

Quadrature Clock Input B. This input has a filter circuit identical to input A.

Mode (Pin 11)

Mode is a 3-state input to select resolutions x1, x2, or x4. The selected resolution multiplies the input quadrature clock rate by 1, 2 and 4 respectively; in producing the outputs UPCK/DNCK and CLK (see Figure 2).

The Mode input logic levels selects resolutions as follows:

Logic 0 = x1 Float = x2 Logic 1 = x4

PIN ASSIGNMENT
TOP VIEW

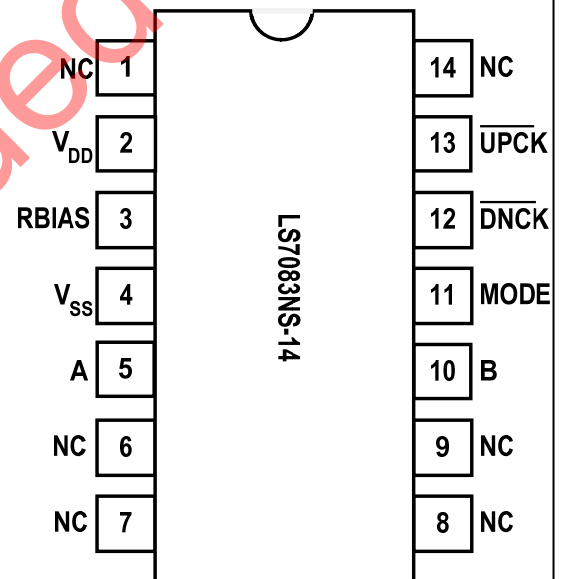


FIGURE 1.

DNCK (Pin 12)

This is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

UPCK (Pin 13)

This is the UP Clock Output. This output consists of low-going pulses generated when A input leads the B input.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	$V_{DD} - V_{SS}$	16.0	V
Voltage at any Input	V_{IN}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:

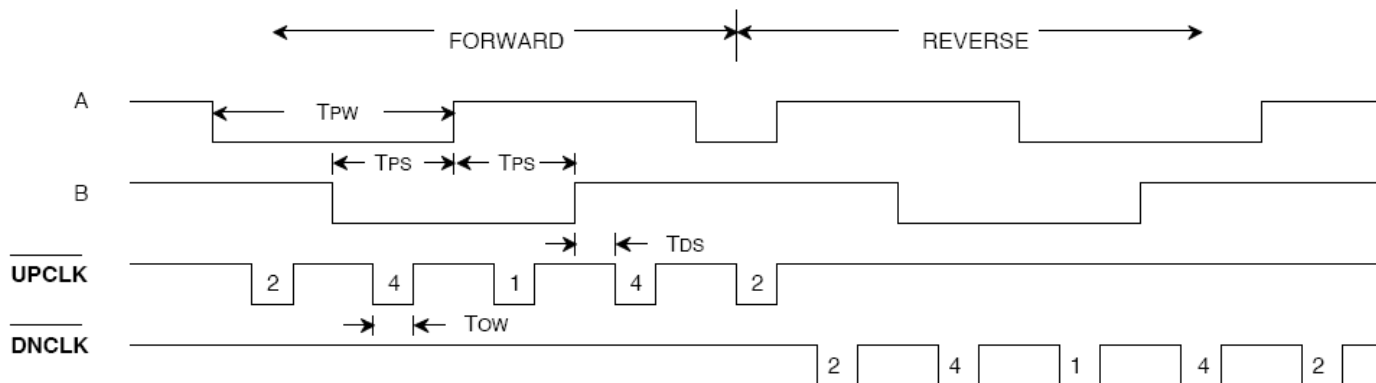
 (All voltages referenced to VSS, $T_A = 0^\circ\text{C}$ to 70°C .)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	3.0	12.0	V	-
Supply Current	I_{DD}	-	100	μA	$V_{DD} = 12\text{V}$, All input frequencies = 0Hz RBIAS = 2M Ω
MODE Logic Low	V_{IL}	-	$0.5V_{DD}$	V	-
A, B Logic Low	V_{IL}	-	0.7	V	$V_{DD} = 3\text{V}$
		-	1.0	V	$V_{DD} = 5\text{V}$
		-	2.8	V	$V_{DD} = 12\text{V}$
MODE Logic High	V_{IH}	$V_{DD} - 0.5$	-	V	-
A, B Logic High	V_{IH}	2.0	-	V	$V_{DD} = 3\text{V}$
		3.0	-	V	$V_{DD} = 5\text{V}$
		6.6	-	V	$V_{DD} = 12\text{V}$
ALL OUTPUTS:					
Sink Current	I_{OL}	1.3	-	mA	$V_{DD} = 3\text{V}$
$V_{OL} = 0.4\text{V}$		1.9	-	mA	$V_{DD} = 5\text{V}$
		2.9	-	mA	$V_{DD} = 12\text{V}$
Source Current	I_{OH}	0.83	-	mA	$V_{DD} = 3\text{V}$
$V_{OH} = V_{DD} - 0.5\text{V}$		1.1	-	mA	$V_{DD} = 5\text{V}$
		1.6	-	mA	$V_{DD} = 12\text{V}$

TRANSIENT CHARACTERISTICS:

 ($T_A = 0^\circ\text{C}$ to 70°C .)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
A,B inputs: Validation Delay	T_{VD}	-	250	ns	$V_{DD} = 3\text{V}$
		-	170	ns	$V_{DD} = 5\text{V}$
		-	71	ns	$V_{DD} = 12\text{V}$
A,B inputs: Pulse Width	T_{PW}	$T_{VD} + T_{OW}$	Infinite	ns	-
A to B or B to A Phase Delay	T_{PS}	T_{OW}	Infinite	ns	-
A,B frequency	$f_{A,B}$	-	$1 / 2T_{PW}$	Hz	-
Input to Output Delay	T_{DS}	-	280	ns	$V_{DD} = 3\text{V}$
		-	220	ns	$V_{DD} = 5\text{V}$
		-	120	ns	$V_{DD} = 12\text{V}$
					Includes input validation delay
Output Clock Pulse Width	T_{OW}	50	-	ns	See Fig. 4 & 5



NOTE: Output clocks labeled 1,2 and 4 have the following interpretations.

1. Generated in x1, x2 and x4 modes.
2. Generated in x2 and x4 modes only.
3. Generated in x4 mode only.

FIGURE 2. LS7083NS-14 INPUT/OUTPUT TIMING

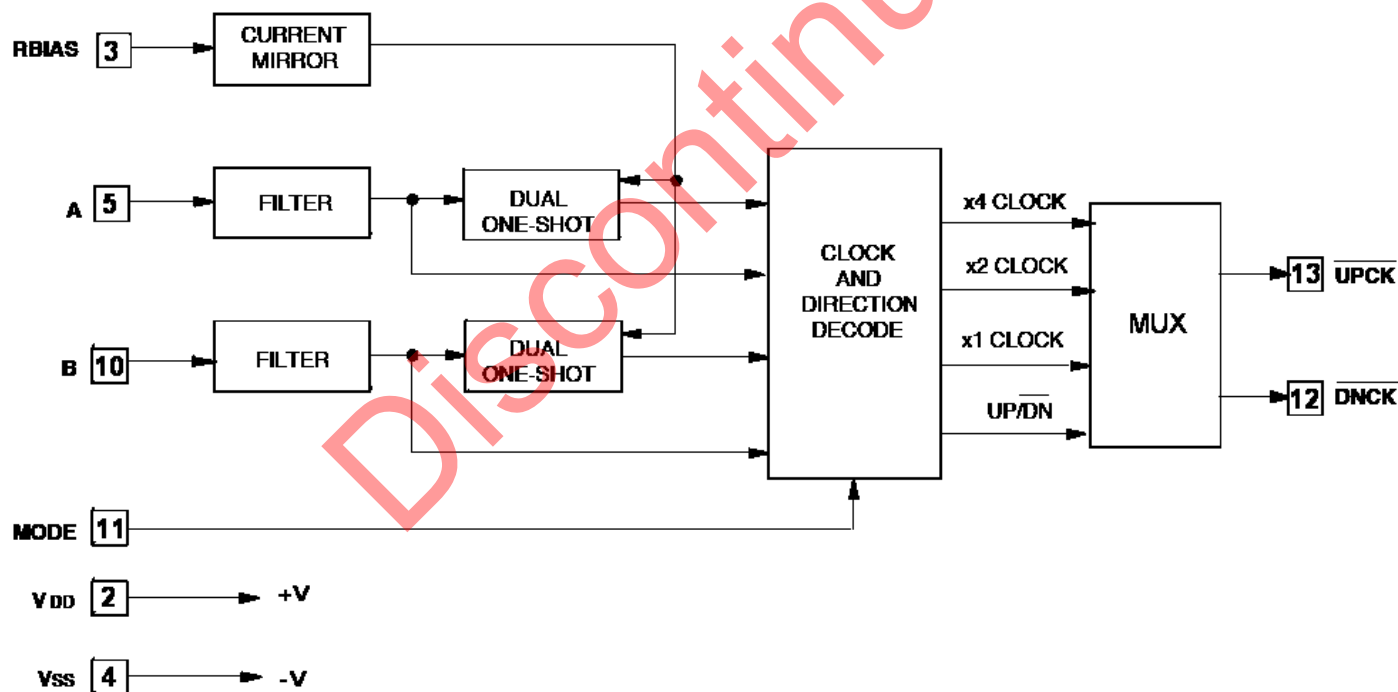


FIGURE 3. LS7083NS-14 BLOCK DIAGRAM

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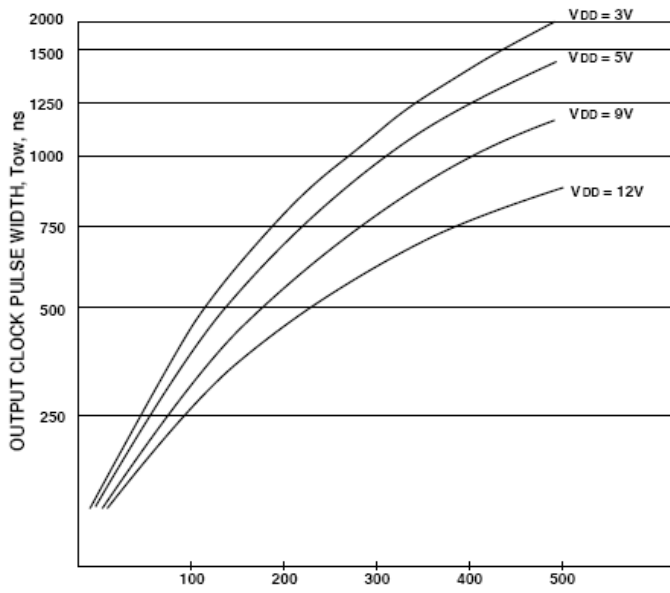


FIGURE 4. T_{ow} vs RBIAS, $k\Omega$

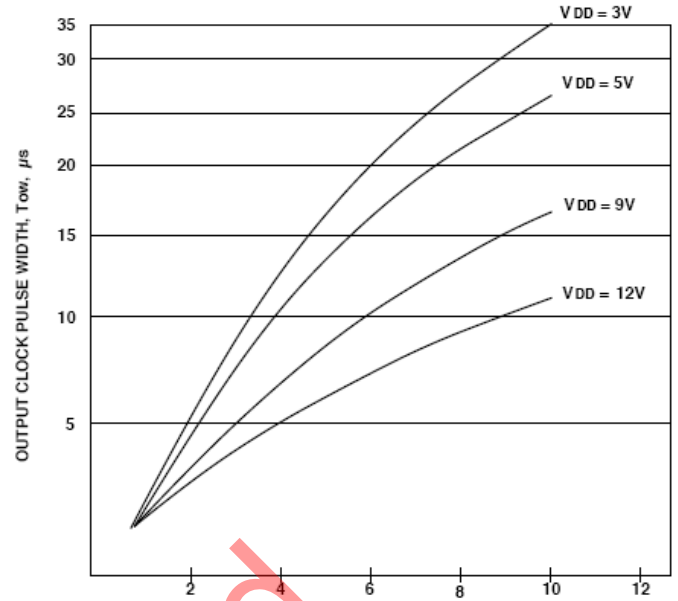


FIGURE 5. T_{ow} vs RBIAS, $M\Omega$

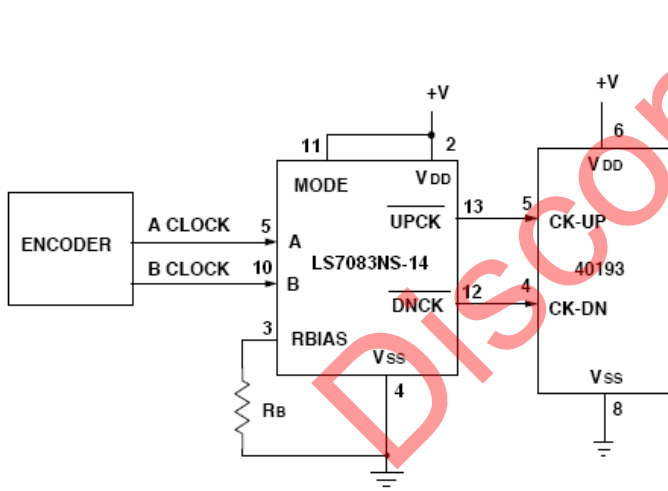


FIGURE 6A. TYPICAL APPLICATION FOR LS7083NS-14 in x4 MODE

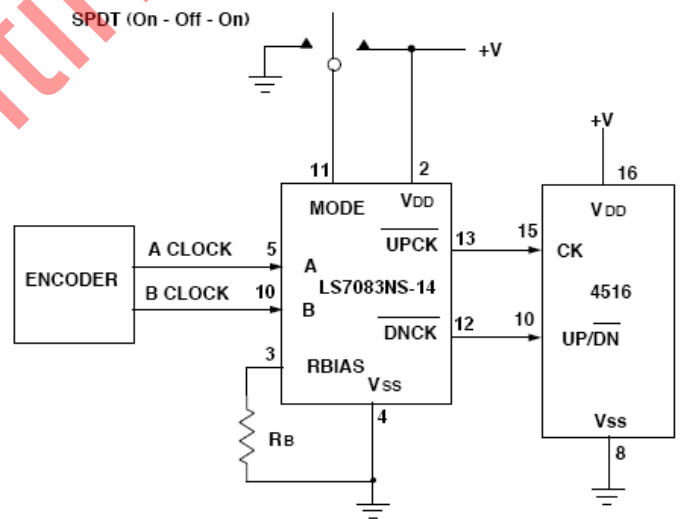


FIGURE 6B. TYPICAL APPLICATION FOR LS7083NS-14 in x2 MODE